CLAIMS

What is claimed is:

1. A method of producing a storage poly structure for a semiconductor capacitor, comprising:

providing a storage poly;

growing a hemispherical-grain polysilicon layer on said storage poly;

applying a mask layer over said hemispherical-grain polysilicon layer;

removing an upper portion of said mask layer to expose elevated portions of said hemispherical-grain polysilicon layer; and

etching through said exposed portions of said hemispherical grain polysilicon layer portions and into said storage poly.

2. The method of claim 1, further comprising:

depositing a photo-resist material on said storage poly to pattern a desired position of said storage poly structure;

etching said storage poly; and

removing said photo-resist material prior to etching through said hemispherical grain polysilicon layer exposed portions.

3. The method of claim 1, wherein providing a storage poly comprises:

depositing a buffer layer on a semiconductor substrate;

patterning a resist material on said buffer layer wherein open areas in said resist material are position in desired areas for formation of said storage poly structure;

etching said buffer layer to expose portions of said semiconductor substrate;

removing said resist material;

applying a layer of polysilicon over said barrier layer wherein said polysilicon layer contacts said semiconductor substrate; and

planarizing said polysilicon layer to the barrier layer forming said storage poly.

4. The method of claim 3, wherein planarizing is performed using a mechanical abrasion.

5. The method of claim 4, wherein said mechanical abrasion is a chemical mechanical planarization process.

6. A method of producing a semiconductor capacitor, comprising:
providing storage poly;
growing a hemispherical-grain polysilicon layer on said storage poly;
applying a mask layer over said hemispherical-grain polysilicon layer;
removing an upper portion of said mask layer to expose elevated portions of said hemispherical-grain polysilicon layer;
etching through said exposed portions of said hemispherical grain polysilicon layer portions and into said storage poly;
depositing a dielectric material over said etched storage poly; and
depositing a cell poly over said dielectric material.

7. The method of claim 6, further comprising:
depositing a photo-resist material on said storage poly to pattern a desired position of said storage poly structure;
etching said storage poly; and
removing said photo-resist material prior to etching through said hemispherical grain polysilicon layer exposed portions.

8. The method of claim 6, wherein providing a storage poly comprises:
depositing a buffer layer on a semiconductor substrate;

patterning a resist material on said buffer layer wherein open areas in said resist material are position in desired areas for formation of said storage poly structure;

etching said buffer layer to expose portions of said semiconductor substrate;

removing said resist material;

applying a layer of polysilicon over said barrier layer wherein said polysilicon layer contacts said semiconductor substrate; and

planarizing said polysilicon layer to the barrier layer forming said storage poly.

9. The method of claim 8, wherein planarizing is performed using a mechanical abrasion.

10. The method of claim 9, wherein said mechanical abrasion is a chemical mechanical planarization process.

11. A method of producing a semiconductor memory cell, comprising:

providing an intermediate structure comprising a semiconductor substrate including at least one field oxide area and at least one active area containing at least one drain region and at least one source region, at least one transistor gate member residing on said substrate active area spanned between said at least one drain region and said at least one source region, and a storage poly which is in contact with the semiconductor substrate;

growing a hemispherical-grain polysilicon layer on said storage poly;

applying a mask layer over said hemispherical-grain polysilicon layer;

removing an upper portion of said mask layer to expose elevated portions of said hemispherical-grain polysilicon layer;

etching through said exposed portions of said hemispherical grain polysilicon layer portions and into said storage poly;

depositing a dielectric material over said etched storage poly; and
depositing a cell poly over said dielectric material.

12. The method of claim 11, wherein said storage poly of said intermediate structure is formed by:

applying a storage poly layer over said at least one field oxide area, said at least one active area, and said at least one transistor gate member;

depositing a photo-resist material on said storage poly to pattern a desired position of said storage poly structure;

etching said storage poly; and

removing said photo-resist material prior to etching through said hemispherical grain polysilicon layer exposed portions.

13. The method of claim 11, wherein said storage poly of said intermediate structure is formed by:

depositing a buffer layer over said at least one field oxide area, said at least one active area, and said at least one transistor gate member;

patterning a resist material on said buffer layer wherein open areas in said resist material are position in desired areas for formation of said storage poly structure;

etching said buffer layer to expose at least a portion of said active area;

removing said resist material;

applying a layer of polysilicon over said barrier layer wherein said polysilicon layer contacts said semiconductor substrate; and

planarizing said polysilicon layer to the barrier layer forming said storage poly.

14. The method of claim 13, wherein planarizing is performed using a mechanical abrasion.

15. The method of claim 14, wherein said mechanical abrasion is a chemical mechanical planarization process.

16. A storage poly structure for a semiconductor capacitor formed by the method comprising:

providing a storage poly;

growing a hemispherical-grain polysilicon layer on said storage poly;

applying a mask layer over said hemispherical-grain polysilicon layer;

removing an upper portion of said mask layer to expose elevated portions of said hemispherical-grain polysilicon layer; and

etching through said exposed portions of said hemispherical grain polysilicon layer portions and into said storage poly.

17. The storage poly structure of claim 16, further comprising:

depositing a photo-resist material on said storage poly to pattern a desired position of said storage poly structure;

etching said storage poly; and

removing said photo-resist material prior to etching through said hemispherical grain polysilicon layer exposed portions.

18. The storage poly structure of claim 16, wherein providing a storage poly comprises:

depositing a buffer layer on a semiconductor substrate;

patterning a resist material on said buffer layer wherein open areas in said resist material are position in desired areas for formation of said storage poly structure;

etching said buffer layer to expose portions of said semiconductor substrate;

removing said resist material;

applying a layer of polysilicon over said barrier layer wherein said polysilicon layer contacts said semiconductor substrate; and

planarizing said polysilicon layer to the barrier layer forming said storage poly.

19. The storage poly structure of claim 18, wherein planarizing is performed using a mechanical abrasion.

20. The storage poly structure of claim 19, wherein said mechanical abrasion is a chemical mechanical planarization process.

21. A semiconductor capacitor produced by the method comprising:

providing storage poly;

growing a hemispherical-grain polysilicon layer on said storage poly;

applying a mask layer over said hemispherical-grain polysilicon layer;

removing an upper portion of said mask layer to expose elevated portions of said hemispherical-grain polysilicon layer;

etching through said exposed portions of said hemispherical grain polysilicon layer portions and into said storage poly;

depositing a dielectric material over said etched storage poly; and

depositing a cell poly over said dielectric material.

22. The semiconductor capacitor of claim 21, further comprising:

depositing a photo-resist material on said storage poly to pattern a desired position of said storage poly structure;

etching said storage poly; and

removing said photo-resist material prior to etching through said hemispherical grain polysilicon layer exposed portions.

23. The semiconductor capacitor of claim 21, wherein providing a storage poly comprises:

depositing a buffer layer on a semiconductor substrate;

patterning a resist material on said buffer layer wherein open areas in said resist material are position in desired areas for formation of said storage poly structure;

etching said buffer layer to expose portions of said semiconductor substrate;

removing said resist material;

applying a layer of polysilicon over said barrier layer wherein said polysilicon layer contacts said semiconductor substrate; and

planarizing said polysilicon layer to the barrier layer forming said storage poly.

24. The semiconductor capacitor of claim 23, wherein planarizing is performed using a mechanical abrasion.

25. The semiconductor capacitor of claim 24, wherein said mechanical abrasion is a chemical mechanical planarization process.

26. A semiconductor memory cell produced by a method comprising:

providing an intermediate structure comprising a semiconductor substrate including at least one field oxide area and at least one active area containing at least one drain region and at least one source region, at least one transistor gate member residing on said substrate active area spanned between said at least one drain region and said at least one source region, and a storage poly which is in contact with the semiconductor substrate;

growing a hemispherical-grain polysilicon layer on said storage poly;

applying a mask layer over said hemispherical-grain polysilicon layer;

removing an upper portion of said mask layer to expose elevated portions of said hemispherical-grain polysilicon layer;

etching through said exposed portions of said hemispherical grain polysilicon layer portions and into said storage poly;

depositing a dielectric material over said etched storage poly; and

depositing a cell poly over said dielectric material.

27. The semiconductor memory cell of claim 26, wherein said storage poly of said intermediate structure is formed by:

applying a storage poly layer over said at least one field oxide area, said at least one active area, and said at least one transistor gate member;

depositing a photo-resist material on said storage poly to pattern a desired position of said storage poly structure;

etching said storage poly; and

removing said photo-resist material prior to etching through said hemispherical grain polysilicon layer exposed portions.

28. The semiconductor memory cell of claim 26, wherein said storage poly of said intermediate structure is formed by:

depositing a buffer layer over said at least one field oxide area, said at least one active area, and said at least one transistor gate member;

patterning a resist material on said buffer layer wherein open areas in said resist material are position in desired areas for formation of said storage poly structure;

etching said buffer layer to expose at least a portion of said active area;

removing said resist material;

applying a layer of polysilicon over said barrier layer wherein said polysilicon layer contacts said semiconductor substrate; and

planarizing said polysilicon layer to the barrier layer forming said storage poly.

29. The semiconductor memory cell of claim 28, wherein planarizing is performed using a mechanical abrasion.

30. The semiconductor memory cell of claim 29, wherein said mechanical abrasion is a chemical mechanical planarization process.

31. A semiconductor capacitor storage poly comprising a plurality of contiguous mesas forming a maze-like structure.

32. The storage poly of claim 31, wherein said mesas extend in the X, Y and Z coordinates.

33. A semiconductor capacitor storage poly comprising a plurality of contiguous webs forming a maze-like structure.

34. The storage poly of claim 31, wherein said webs extend in the X, Y and Z coordinates.